CLAIMS

What is claimed is:

1. A data transfer block for use in an integrated circuit (IC) to interface an on-chip subsystem to an on-chip bus, the data transfer block comprising:

a first and a second outbound queue to facilitate selective staging of a first and a second plurality of outbound bus transactions for the on-chip subsystem, at the choosing of the on-chip subsystem, each of said outbound bus transactions including a bus arbitration priority; and

a first state machine coupled to the first and second outbound queues to service the first and second outbound queues, serially requesting for access to the on-chip bus for the staged outbound bus transactions, according the first queue a first outbound priority and the second queue a second outbound priority, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions.

2. The data transfer block of claim 1, wherein said data transfer block further comprises a configuration register coupled to said first state machine to store said first and second priorities to be accorded to said first and second outbound queues by said first state machine in servicing said first and second outbound queues.

3. The data transfer block of claim 1, wherein

the data transfer block further comprises a third outbound queue, which in conjunction with said first and second outbound queues, facilitates selective staging of a third and said first and second plurality of outbound bus transactions for the on-chip subsystem, at the choosing of the on-chip subsystem, with each of the outbound bus transactions including a bus arbitration priority; and

said first state machine is also coupled to said third outbound queue, and service said third outbound queue, along with said first and second outbound queues, serially requesting for access to the on-chip bus for the staged outbound bus transactions, according the third queue a third outbound priority complementing said first and second outbound priorities accorded to the first and second outbound queues, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions.

4. The data transfer block of claim 1, wherein the data transfer block further comprises

a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

a second state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority.

5. The data transfer block of claim 4, wherein said data transfer block further comprises a configuration register coupled to said second state machine to store said first and second inbound priorities to be accorded to said first and second inbound queues by said second state machine in servicing said first and second inbound queues.

6. The data transfer block of claim 1, wherein

the data transfer block further comprises a third inbound queue, which in conjunction with said first and second inbound queues, facilitates selective staging of a third and said first and second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, with each of the inbound bus transactions including a bus arbitration priority, and granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

said second state machine is also coupled to said third inbound queue, and service said third inbound queue, along with said first and second inbound queues,

serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem, according the third queue a third inbound priority complementing said first and second inbound priorities accorded to the first and second inbound queues.

7. A data transfer block for use in an integrated circuit (IC) to interface an on-chip subsystem to an on-chip bus, the data transfer block comprising:

a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

a state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority.

8. The data transfer block of claim 7, wherein said data transfer block further comprises a configuration register coupled to said state machine to store said first and second inbound priorities to be accorded to said first and second inbound queues by said state machine in servicing said first and second inbound queues.

9. The data transfer block of claim 7, wherein

the data transfer block further comprises a third inbound queue, which in conjunction with said first and second inbound queues, facilitates selective staging of a third and said first and second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, with each of the inbound bus transactions including a bus arbitration priority, and granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

said state machine is also coupled to said third inbound queue, and service said third inbound queue, along with said first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem, according the third queue a third inbound priority complementing said first and second inbound priorities accorded to the first and second inbound queues.

10. A subsystem of an integrated circuit, the subsystem comprising:

core subsystem logic; and

a data transfer unit to couple the core subsystem logic to an on-chip bus of the integrated circuit, the data transfer unit including

a first and a second outbound queue to facilitate selective staging of a first and a second plurality of outbound bus transactions for the core subsystem logic, at the choosing of the core subsystem logic, each of said outbound bus transactions including a bus arbitration priority; and

a first state machine coupled to the first and second outbound queues to service the first and second outbound queues, serially requesting for access to the on-chip bus for the staged outbound bus transactions, according the first queue a first outbound priority and the second queue a second outbound priority, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions.

11. The subsystem of claim 10, wherein said data transfer unit further comprises a configuration register coupled to said first state machine to store said first and second priorities to be accorded to said first and second outbound queues by said first state machine in servicing said first and second outbound queues.

12. The subsystem of claim 10, wherein

the data transfer unit further comprises a third outbound queue, which in conjunction with said first and second outbound queues, facilitates selective staging of a third and said first and second plurality of outbound bus transactions for the core subsystem logic, at the choosing of the core subsystem logic, with each of the outbound bus transactions including a bus arbitration priority; and

said first state machine is also coupled to said third outbound queue, and service said third outbound queue, along with said first and second outbound queues, serially requesting for access to the on-chip bus for the staged outbound

bus transactions, according the third queue a third outbound priority complementing said first and second outbound priorities accorded to the first and second outbound queues, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions.

13. The subsystem of claim 12, wherein the data transfer unit further comprises

a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for the core subsystem logic, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

a second state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the core subsystem logic, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority.

14. The subsystem of claim 13, wherein said data transfer block further comprises a configuration register coupled to said second state machine to store said first and second inbound priorities to be accorded to said first and second

inbound queues by said second state machine in servicing said first and second inbound queues.

15. The subsystem of claim 10, wherein

the data transfer block further comprises a third inbound queue, which in conjunction with said first and second inbound queues, facilitates selective staging of a third and said first and second plurality of inbound bus transactions for the core subsystem logic, at the choosing of originating subsystems of the inbound bus transactions, with each of the inbound bus transactions including a bus arbitration priority, and granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

said second state machine is also coupled to said third inbound queue, and service said third inbound queue, along with said first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the core subsystem logic, according the third queue a third inbound priority complementing said first and second inbound priorities accorded to the first and second inbound queues.

16. The subsystem of claim 10, wherein the subsystem is a selected one of a memory controller, a security engine, a voice processor, a collection of peripheral device controllers, a framer processor, and a network media access controller.

17. A subsystem of an integrated circuit, the subsystem comprising:

core subsystem logic; and

a data transfer unit to couple the core subsystem logic to an on-chip bus of the integrated circuit, the data transfer unit including

a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for the core subsystem logic, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

a state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the core subsystem logic, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority.

18. The subsystem of claim 17, wherein said data transfer unit further comprises a configuration register coupled to said state machine to store said first and second inbound priorities to be accorded to said first and second inbound queues by said state machine in servicing said first and second inbound queues.

19. The subsystem of claim 17, wherein

the data transfer block further comprises a third inbound queue, which in conjunction with said first and second inbound queues, facilitates selective staging of a third and said first and second plurality of inbound bus transactions for the core subsystem logic, at the choosing of originating subsystems of the inbound bus transactions, with each of the inbound bus transactions including a bus arbitration priority, and granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

said state machine is also coupled to said third inbound queue, and service said third inbound queue, along with said first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the core subsystem logic, according the third queue a third inbound priority complementing said first and second inbound priorities accorded to the first and second inbound queues.

20. The subsystem of claim 17, wherein the subsystem is a selected one of a memory controller, a security engine, a voice processor, a collection of peripheral device controllers, a framer processor, and a network media access controller.

21. In a subsystem of an integrated circuit, a method of operation comprising:

determining intra-subsystem priorities for transactions with others subsystems of the integrated circuit to be serviced for requesting access to an on-chip bus of the integrated circuit, to which the subsystems are coupled;

generating and staging the transactions in accordance with the determined intra-subsystem priorities, including with each of the staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip bus with other inter-subsystem transactions of other subsystems of the integrated circuit; and

serially servicing the staged transactions in accordance with their intra-subsystem priorities, requesting access to the on-chip bus for each staged transaction being serviced using the included bus arbitration priority.

22. The method of claim 21, wherein said generating and staging comprises generating and staging each of the transactions in a selected one of a plurality of outbound queues in accordance with the determined intra-subsystem priorities, including with each of the staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip bus with other inter-subsystem transactions of other subsystems of the integrated circuit.

23. The method of claim 21, wherein the method further comprises

staging transactions from other subsystems in a priority based manner as requested by originating subsystems of the transactions, each of said transactions from other subsystems having a bus arbitration priority, on which access to a on-chip bus was granted; and

serially servicing the staged transactions from other subsystems, notifying core logic of the subsystem, in accordance with the priority based manner the transactions from other subsystems are staged.

24. The method of claim 23, wherein said staging of transactions from other subsystems comprises staging each of the transactions from other subsystems in a selected one of a plurality of prioritized inbound queues as requested by the originating subsystems of the transactions.

25. In a subsystem of an integrated circuit, a method of operation comprising:

staging transactions from other subsystems in a priority based manner as requested by originating subsystems of the transactions, each of said transactions from other subsystems having a bus arbitration priority, on which access to a on-chip bus the subsystems are coupled was granted; and

serially servicing the staged transactions from other subsystems, notifying core logic of the subsystem, in accordance with the priority based manner the transactions from other subsystems are staged.

26. The method of claim 25, wherein said staging of transactions from other subsystems comprises staging each of the transactions from other subsystems in a selected one of a plurality of prioritized inbound queues as requested by the originating subsystems of the transactions.

27. An integrated circuit comprising:

an on-chip bus; and

a plurality of subsystems coupled to the on-chip bus and interact with each other through transactions conducted across said on-chip bus, with each of the subsystems having a data transfer interface that interfaces the subsystem to the on-chip bus, and at least one of the data transfer interfaces allows the particular subsystem to initiate transactions with other subsystems in a prioritized manner, including a first intra-subsystem prioritization on the order transactions contending for the service of the at least one of the data transfer interfaces are to be serviced, and a second inter-subsystem prioritization on the order transactions of the various subsystems contending for the on-chip bus are to be granted access to the on-chip bus.

28. The integrated circuit of claim 27, wherein the at least one of the data transfer interfaces comprises

a first and a second outbound queue to facilitate selective staging of a first and a second plurality of outbound bus transactions for the particular subsystem, at the choosing of core logic of the particular subsystem, with each of said outbound bus transactions including a bus arbitration priority; and

a first state machine coupled to the first and second outbound queues to service the first and second outbound queues, serially requesting for access to the

on-chip bus for the staged outbound bus transactions, according the first queue a first outbound priority and the second queue a second outbound priority, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions.

29. The integrated circuit of claim 28, wherein the at least one of the data transfer interfaces further comprises

a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for core logic of the particular subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

a second state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the core logic of the particular subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority.

30. The integrated circuit of claim 27, wherein the at least one of the data transfer interfaces comprises

a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for core logic of the particular subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority; and

a state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the core logic of the particular subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority.

31. The integrated circuit of claim 27, wherein the subsystems are selected ones of a memory controller, a security engine, a voice processor, a collection of peripheral device controllers, a framer processor, and a network media access controller.

32. In an integrated circuit having an on-chip bus and a plurality of subsystems coupled to each other via the on-chip bus, a method of operation comprising:

a first subsystem having a first data transfer interface interfacing the first subsystem to the on-chip bus, initiating first transactions with other subsystems through selective employment of facilities of the first data transfer interface to

internally prioritizing the order the first transactions are to be serviced by the first data transfer interface, and including with said first transactions first bus arbitration priorities to facilitate prioritization of granting of access to the on-chip bus to contending inter-subsystem transactions including said first transactions; and

a second subsystem having a second data transfer interface interfacing the second subsystem to the on-chip bus, initiating second transactions with other subsystems through selective employment of facilities of the second data transfer interface to internally prioritizing the order the second transactions are to be serviced by the second data transfer interface, and including with said second transactions second bus arbitration priorities to facilitate prioritization of granting of access to the on-chip bus to contending inter-subsystem transactions including the second transactions.

33. The method of claim 32, wherein the method further comprises the first data transfer interface of the first subsystem staging third transactions from other subsystems in a priority based manner as requested by originating subsystems of the third transactions, said third transactions from other subsystems also having third bus arbitration priorities, based on which accesses to said on-chip bus were granted;

34. The method of claim 33, wherein the method further comprises the first data transfer interface of the first subsystem serially servicing the staged third

transactions from other subsystems, notifying core logic of the first subsystem, in accordance with the priority based manner the third transactions from other subsystems are staged.

35. The method of claim 33, wherein the method further comprises the second data transfer interface of the second subsystem staging fourth transactions from other subsystems in a priority based manner as requested by originating subsystems of the fourth transactions, said fourth transactions from other subsystems also having fourth bus arbitration priorities, based on which accesses to said on-chip bus were granted.